VARIABLE STAGE CHARGE PUMP

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to variable stage charge pumps, and, more specifically, to a charge pump that has a selectable number of stages.

Description of the Related Art

In some electronic devices, the power supply voltage is not high enough to guarantee the correct operation of the circuit. In these cases, higher voltages are required. For example, voltages up to 15 volts are needed for programming and erasing operations in a non-volatile memory device.

When a voltage higher than the power supply voltage is required, a second power supply can be furnished from outside the circuit. Until a few years ago, this was the only solution available. Presently, the required voltages can be also generated inside the integrated circuit. On-circuit high voltage generation is now more widespread than off-chip generation, because of lower implementation cost.

A circuit that can provide higher voltage values than the power supply is typically called a charge pump.

Figure 1 shows, in a simplified manner, an N-stage charge pump 10, each stage comprising a switch 12 and a pumping capacitor 14. Additionally a load capacitance 16 and a load current 18 are shown. The integration area of the charge pump is very large and it increases when the current output must be high.

The current output from a charge pump can be determined as follows:

$$I_L = \frac{(N+1)\cdot V_{dd} - V_{OUT}}{N^2} \cdot C_{TOT} \cdot f \qquad (1)$$

where,

N is the number of charge pump stages;

Vdd is the power supply voltage;

Vout is the output voltage;

C_{TOT} is the total capacitance value of all pumping capacitors; and

f is the switching frequency.

In order to make the output current equal to the current required by the load, the pumping frequency, f, is varied from 0 Hz to f_{MAX}.

Therefore, the maximum current value for an N-stage charge pump is:

$$I_{LMAX} = \frac{(N+1)\cdot V_{dd} - V_{OUT}}{N^2} \cdot C_{TOT} \cdot f_{MAX} \qquad (2)$$

The power supply voltage Vdd can be of any value within a given fixed range. The output voltage Vout is related to the load driven in a given time by the charge pump. The capacitors that make up C_{TOT} require the largest part of the integration area of the charge pump

In order to maximize the current output from the charge pump, with the same amount of occupied area (and thus the same C_{TOT}) and with the same maximum frequency, f_{MAX}, the number of stages N can be opportunely chosen.

As described in *Optimization of Word-Line Booster Circuits for Low-Voltage Flash Memories* – IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, August 1999, the number of stages N for which the current output has the maximum value is:

$$N_{OPT} = 2 \cdot \left(\frac{V_{OUT}}{V_{dd}} - 1 \right) \qquad (3)$$

As seen from equation 3, the number of stages is dependent on the power supply voltage, Vdd, and the output voltage V_{OUT}. The supply voltage may not be known at the time the charge pump is designed, and output voltage, V_{OUT} have different requirements at different times, for example in order to drive different loads. Both of these

unknown values makes it difficult to accurately design a suitably sized charge pump. If the number of stages chosen is too few, the necessary output current may not be able to be achieved; if the number of stage chosen is too many, valuable integrated circuit area (for the unnecessary extra capacitors) is wasted.

SUMMARY OF THE INVENTION

Embodiments of the invention are directed to a charge pump that has a variable number of stages. This allows the output current to be maximized for a given integration area by selecting the number of stages to use in the charge pump. Additionally, embodiments of the invention allow the charge pump to be reconfigured if the power supply voltage or the output voltage specifications change.

Presented is a variable stage charge pump that includes a number of individual units. Each of the units has a number of switch and capacitor circuits coupled between an input terminal and an output terminal to make up the individual unit. Additionally, the charge pump includes a switching network that can be selected to combine different individual units of the charge pump so that they can work in either a parallel mode or a serial mode. In some embodiments, the switching network is made by switches with connections that can be kept open during a pumping operation. Some embodiments include a switching network made from a switched diode. A method of driving the charge pump and the switching network is also presented.

The invention can be embodied in many different ways. The following figures and description explain the invention with reference to different embodiments thereof, but the invention is not limited to those embodiments shown.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a schematic diagram of a charge pump according to the prior art.

Figure 2 is a schematic diagram of an example charge pump according to an embodiment of the invention.

Figure 3A is a schematic diagram showing states of an example switch network of the charge pump shown in Figure 2.

Figure 3B is a chart showing the phases of the switches shown in Figure 3A.

Figure 4A is a schematic diagram showing states of an example switch network of the charge pump shown in Figure 2.

Figure 4B is a chart showing the phases of the switches shown in Figure 4A.

Figure 5A is a schematic diagram showing states of an example switch network of the charge pump shown in Figure 2.

Figure 5B is a chart showing the phases of the switches shown in Figure 5A.

Figure 6 is an example block diagram of a circuit including a charge pump according to an embodiment of the invention and other sub-circuits used in conjunction with the charge pump.

Figure 7 is an example block diagram of a circuit including a charge pump according to an embodiment of the invention and other sub-circuits used in conjunction with the charge pump.

Figure 8 is a block and schematic diagram of an example phase assigner shown in Figure 7.

Figure 9 is a graph showing how the number of phases in the charge pump is preferably assigned.

Figure 10A is a schematic diagram of an example embodiment of the optimal stages finder shown in Figure 7.

Figure 10B is a chart showing the outputs of the optimal stages finder shown in Figure 10A.

Figure 11 is a schematic diagram of a charge pump according to the prior art.

Figure 12 is a detailed schematic diagram of the charge pump of Figure 11.

Figure 13 is a schematic diagram of coupled charge pumps according to the prior art.

Figure 14 is a schematic diagram of coupled charge pumps according to an embodiment of the invention.

Figure 15 is a detailed schematic diagram of circuits contained in the charge pumps of Figure 14.

Figure 16 is a timeplot of output from a realized version of the charge pump of Figure 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to embodiments of the invention, a variable stage charge pump can be obtained by dividing the total capacitance, C_{TOT}, from equations 1 and 2, into a suitable number of pumping capacitors, and connecting these pumping capacitors together through a suitable switching network. The switching network acts on the frequencies of the pumping capacitors and on the frequency of the switching drivers to decide the appropriate number of stages in the charge pump.

Figure 2 is a schematic diagram of an example charge pump 50 according to an embodiment of the invention. The charge pump 50 includes between 1 and 3 stages, depending on a configuration of its switching network. The charge pump 50 includes a number of switches 20, individually labeled T1 – T17, and a number of capacitors 24, individually labeled F1 – F6. Each of the switches 20 is individually controllable to either an open or shut position, although they are all shown in Figure 2 as being open. Also included in the charge pump 50 are the power supply voltage Vdd and the output load capacitance 16 and current 18.

The charge pump 50 is shown in Figure 3A with the switches T7, T8, T9, T10, and T11 fixed open (no arrow through the switch symbol). The remaining switches 20 are switchable either to an open or closed position by an appropriate signal in an appropriate phase. If the capacitors F1 – F6 and the remaining switches 20 in Figure 3 are driven by means of the phase values according to Figure 3B, the charge pump 50 works as a charge pump having a single stage of 6 parallel charge pumps. The phase diagram of Figure 3B can be explained as follows. An "F" representation in the boxes marked F1 – F6

means that an in-phase signal is provided to the open terminal of the respective capacitors F1 – F6. An "F" representation in the boxes marked F_{T1} – F_{T17} means that an in-phase signal is provided to the switches T1 – T17, and causes them to close. Conversely, an $\overline{F}$ symbol in the respective box means that the open terminal of the respective capacitor is driven with an out of phase signal, or that the switch is driven to an open position. As stated above, with the charge pump 50 of Figure 3A driven with the phases as shown in Figure 3B, results in a single stage, 6-parallel pump charge pump.

The same charge pump 50 is shown in Figure 4A with a different configuration. In that figure, switches T1, T3, T5, T8, T10, T12, T14 and T16 are held open, while the remainder are driven by the phase signals as shown in Figure 4B. In this configuration, with the phase signals as shown in Figure 4B, the charge pump 50 operates as a charge pump having two stages, with 3 charge pumps in parallel.

The same charge pump 50 is shown in Figure 5A with a still a different configuration. In that figure, switches T1, T3, T5, T6, T9, T12, T13, T14, and T16 are held open, while the remainder are driven by the phase signals as shown in Figure 5B. In this configuration, with the phase signals as shown in Figure 5B, the charge pump 50 operates as a charge pump having three stages, with 2 charge pumps in parallel.

A charge pump with fixed or variable stages cannot work alone, and requires other circuitry for correct operation, for instance a control circuit. Figure 6 is an example block diagram of a circuit 60 including a charge pump 50 and other sub-circuits to ensure the correct operation of the charge pump. The circuit 60 includes a clock generator 62, a phase generator 64, which provides the required phases to drive the switches and the pumping capacitors in the charge pump 50, and a V_{OUT} regulator 66, which maintains the output voltage at a fixed value in the best possible way.

A charge pump having variable stages needs two additional circuits, as shown in the block diagram of Figure 7, given by way of an example. In Figure 7, a circuit 70 includes the clock generator 62, the phase generator 64 and the output voltage regulator 66 as in the circuit 60 of Figure 6. Additionally the circuit 70 includes a phase assigner 72, which assigns the phases generated by the phase generator 64 to the switches and pumping

capacitors in the charge pump 50 such that the charge pump has the desired number of stages. Further, the circuit 70 includes an optimal stages finder 74, which uses the power supply voltage, Vdd, and the output voltage, V_{OUT} (or a regulation voltage, V_{REG}), received at its inputs, and provides the number of stages N which guarantees the maximum output current from the circuit 70.

The phase assigner 72 can be made, for example, by several multiplexers 76. A preferred embodiment includes the same number of multiplexers 76 as there are capacitors and switches to be driven in the charge pump 50, as shown with reference to Figure 8. Each multiplexer 76 receives, as input, a signal for the number of phase conditions that can be used, in this case F and $\overline{F}$. Additionally, the multiplexer 76receives a selection, N, that determines which phases will be passed on to the capacitors and switches to be driven in the charge pump 50.

Using the equation (3), it is possible to define the optimal number of stages when the $\frac{V_{OUT}}{V_{dd}}$ rate varies, as shown, in Figure 9. That figure shows the supply voltage V_{dd} varying between 1.5 and 3.7 V, and V_{OUT} = 5V. From Figure 9, it is clear that knowing the $\frac{V_{OUT}}{V_{dd}}$ ratio with respect to 1.5 and 2.0 allows the optimal value of N to be obtained. As seen in the figure, if the ratio is less than 1.5, the optimal value of N is 1; if the ratio is between 1.5 and 2, the optimal value of N is 2, and if the ratio is over 2, the optimal value of N is 3.

A possible embodiment of the optimal stages finder 74 is shown in Figure 10A. In that embodiment, the optimal stages finder includes a first and a second comparator, 82 and 84, which have their inverting inputs tied together and to a resistor ladder 88. Non-inverting inputs of the comparators are coupled to different nodes in a second resistor ladder 90. The resistor ladder 88 is coupled to the Vdd power supply voltage, while the resistor ladder 90 is coupled to the Vreg, the regulating voltage shown in Figure 7.

A logic circuit 94 is coupled to the output of the comparators 82 and 84, and is structured to output the optimum value for N, either 1, 2 or 3, in a value composed of the signals on the lines N1 and N0, according to the table shown in Figure 10B.

A further embodiment of a charge pump having a variable number of stages is shown in Figures 11 - 16. In Figure 11, a basic charge pump 100 is shown, similar to the one shown in Figure 1. However, diodes 102 have been substituted where there were switches 12 in Figure 1. Pumping capacitors 104 are also included in the charge pump 100, as well as a load capacitor 106.

A more detailed schematic diagram of the charge pump 100 is shown in Figure 12. In that diagram, a charge pump 110 replaces the diodes 102 of Figure 11 with a switched diode structure 112. These switched diodes 112 have only a very small voltage drop, on the order of tens of mV, instead of hundreds of mV as for a simple diode illustrated in Figure 11.

In Figure 12, the transistors T1 and T2 that make up the switched diode structure 112 are natural MOS transistors having a very low threshold (about 100mV). In this way, the final stages do not reach threshold voltages comparable to Vdd, because of the body effect.

The transistor T1 is suitably sized in such a way to let flow all of the current to be transferred in a half-clock-period and to provide for a V_{DS} that is as small as possible. Transistor T2 is used to switch T1 in the inverse diode configuration when the following stage is boosted. Although Figure 12 only shows one switched diode structure 112 outright, additional switched diode structures are shown by implication. Compared to Figure 11, in the charge pump 110, each of the diodes 102 are replaced by the switched diode structure 112, except for the first and last diodes 102, which have special functions in the embodiment of the charge pump 110, as described herein.

Also included in the charge pump 110 of Figure 12 are a number of boost capacitors 114. The boost capacitors 114 are suitably sized in such a way to provide for a transferring of the 90% of the voltage difference provided by a signal FN, and thus

provides a correct "overdrive" to the transistor T1 of the switched diode structures 112 during a charge transferring phase.

The FN phase signal is made at a double voltage value with respect to the F phase signal of Figure 11, for the voltage on T1, $V_{GS}>>Vt$.

With respect to the connection to Vdd, the charge pump 110 includes a structure 111, and does not need a complete switched diode structure 112 there. Since the booster first node varies from Vcc to 2Vcc, the structure 111 only requires an additional diode T0 and, in order to gain a value equal to its threshold voltage, transistor T1 is driven by FN phase, in such a way to force diode operation in the inverted configuration.

On the contrary, the output stage is provided with an auxiliary structure, which emulates a subsequent stage in order to guarantee the switching-on of the transistor T2 during the phase, which follows the charge transferring to the output. The auxiliary structure includes a third transistor, T3 coupled between the capacitor Cb 114 and the stage before the output stage, as shown in Figure 12.

Two or more charge pumps 110 can be connected in parallel in order to increase the driving capability. Generally speaking, two charge pumps operating with opposite phases are connected in parallel, in such a way that they alternatively provide an output current, with the additional advantage of doubling the output current and greatly reducing the required size of capacitor Cout for a same ripple.

Figure 13 shows an example of two charge pumps 110 operating with opposite phases and connected in parallel. Since the area required by each charge pump 110 is not negligible, it is possible to share the functions of two charge pumps. In one configuration, two charge pumps are configured in a parallel fashion, to create a low regulation voltage having a high driving capability. Also, two charge pumps can be configured in a serial fashion for a high regulation voltage having a low driving capability.

Figure 14 shows the basic operation scheme of a FP1 and FP2 correspond to the boosted phases, FN1 and FN2, for the parallel configuration, while they correspond to FS1 and FS2 for 0V. The charge pump of Figure 14 differs from the prior art ones discussed with reference to Figures 11 and 12. Specifically, the charge pump 120 includes

a Vdd connecting circuit 122, an output circuit 124, and an interconnection circuit 126. Detail of those circuits is shown in Figure 15.

In the output circuit 124, the switch diodes TP2 and TP3, which correspond to the transistors T2 and T3 in Figure 12, have a circuit structure as shown in Figure 15. With respect to the known structures for switch diodes 116, suitable HV MOS transistors have been substituted, which have a high threshold (600mV) in order to guarantee the complete switching-off of the structure, the operation during the on-phase being the same. This avoids having paths to ground throughout the low threshold transistors. The size of the transistors TP do not excessively charge the capacitors Cb.

As for the control signals that drive the circuits 126, 122 and 124, the control signal ENP is equal to the output voltage of the charge pump when the charge pump 120 is in the parallel configuration, while it is equal to zero when the charge pump is in the serial configuration. The control signal ENS has opposite signals. The signal ENL is equal to Vcc according to the parallel configuration, while it is equal to zero according to the serial configuration.

When in parallel configuration, signals ENL and ENP are high, while signals ENS, FS1 and FS2 are low. In this way, transistors T0 and TS2 are on, while transistors TP and TS1 are off. The TS1 switching-off guarantees the path-to-ground cut, since T2 and TS2 are on. The TS2 switching-on guarantees the T1 switching-off and thus the serial-path cut. The type of the transistors TS2 and TS3 does not affect the operating with respect to the structure comprising low threshold transistors, if they work with sufficient low voltages, but, according to their definition, they provide for a good overdrive of TS2 and TS3 for the voltages used in the parallel configuration.

In the serial configuration, the signal ENS is high, while signals ENL, ENP, FP1 and FP2 are low. In this way, transistors TS1 and TP are on, while transistors T0 and TS0 are off. Transistor TS1 shows an high overdrive, since it is driven by the output voltage of the charge pump and the voltage values at its ends are, in any case, lower for at least one stage. Also voltage values at the ends of TS2 are, in any case, well lower than the

breakdown threshold. The switching-on of transistors TP guarantees the switching-off of transistors T1, TP2 and TP3 and thus the parallel-path cut.

The limits of the charge pump 120 are essentially due to the technology, which forces the threshold and breakdown voltages of the transistors. Additionally, there are limits on the power supply voltage Vdd and on the number of stages that can be formed.

A configurable booster has been formed in F6Y technology ($1.8V<Vcc>3.6V$ - Vb_{HV} = 17V) and the following performance have been obtained for Vcc = 2.3V and f = 10 MHz.

Parallel: V_{out} = 5.5V; I_{out} = 240uA

Serial: V_{out} = 15V; I_{out} = 60uA

The known solution, according to equation (3) above, has the following results for the above-listed two cases:

1) n = 3 - Cp= 20pF;

2) n = 12 - Cp = 5pF;

The proposed solution can accomplish this by using only 5 pF capacitors, by changing when the charge pump 120 is operating in serial or parallel fashion, as can be seen with reference to Figure 14.

In that figure, when the configuration is operating in parallel (to produce the lower output voltage with high driving capability), four boosters (each of the four lines) with three stages (three pumping capacitors 104) are needed, two by two operating in phase opposition. When the higher voltage is desired, the charge pump 120 can operate in serial mode, only one booster with 12 stages. In that configuration, the output of the first line (at the bottom of the figure) is passed to the input of the line above it, and so on, until the output from the top line is the output of the charge pump that is delivered to the output load.

The simulation results for a fabricated charge pump, for Vcc=2.3V, f=10MHz and T=27°C condition, are shown in Figure 16.

The operating of such a circuit is guaranteed for the whole range for the power supply voltage allowed in technology F6Y, with frequencies less or equal than 20MHz and temperature between -40°C and 125°C, showing a maximum loss, in the worst conditions, equal to 10% of its driving capability.

Changes can be made to the invention in light of the above detailed description. In general, in the following claims, the terms used should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims, but should be construed to include all methods and devices that are in accordance with the claims. Accordingly, the invention is not limited by the disclosure, but instead its scope is to be determined by the following claims.